

REMARKS

Claims 1-20 are pending. Applicant gratefully acknowledges the Examiner's indication that claims 4, 6 - 12, and 14 - 20 contain allowable subject matter. However, Applicant respectfully traverses the rejection of the remaining claims.

In that regard, Applicant has amended claim 1 such that the programmable logic block includes "a plurality of macrocells, the macrocells operable to provide logical outputs at the block's output terminals from logical inputs received at the block's input terminals." Thus, the logical outputs processed by the hardwired microsequencer set forth in claim 1 are provided by the plurality of macrocells.

The Agrawal reference (USP 5,042,004) stands in sharp contrast to the programmable logic device recited in claim 1. For example, Figure 1 of the Agrawal reference shows that the macrocell (within element 160) does not provide any inputs to the stack (element 130). Thus, the macrocells in the Agrawal reference can thus store no state information. In sharp contrast, these elements in claim 1 are providing logical outputs to the hardwired microsequencer and can thus store state information, if such a storage is desired. A user of the Agrawal device has no such option. Accordingly, claim 1 and its dependent claims 2 - 8 are allowable over the Agrawal

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reference. Claim 2 has been amended in light of the change to claim 1. In addition, claim 5 has been amended to clarify the antecedent basis and number of "logical inputs" provided by the memory.

Claim 13 has been amended analogously to the amendment of claim 1. Thus, claim 13 is also allowable over the Agrawal reference.

In addition, claim 18 has been amended to address the minor typographical error noted by the Examiner. Moreover, the specification has also been amended to address a few other typographical errors. No new matter is added.

Accordingly, claims 1 - 20 are in condition for allowance.

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Respectfully submitted,



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